(FILE 'USPAT' ENTERED AT 09:04:25 ON 28 AUG 1998)
7 SEA FLOATING GATE (P) (SIC OR SILICON CARBIDE)

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L1

- 1. 5,798,548, Aug. 25, 1998, Semiconductor device having multiple control gates; Hideaki Fujiwara, 257/319, 321 [IMAGE AVAILABLE].
- 2. 5,754,477, May 19, 1998, Differential flash memory cell and method for programming; Leonard Forbes, 365/185.33, 189.01 [IMAGE AVAILABLE]
- 3. 5,740,104, Apr. 14, 1998, Multi-state flash memory cell and method for programming single electron differences; Leonard Forbes, 365/185.03, 45, 185.28, 185.33 [IMAGE AVAILABLE]
- 4. 5,629,222, May 13, 1997, Method of forming semiconductor memory device by selectively forming an insulating film on the drain region; Shunpei Yamazaki, et al., 438/259, 261, 264 [IMAGE AVAILABLE]
- 5. 5,449,941, Sep. 12, 1995, Semiconductor memory device; Shunpei Yamazaki, et al., 257/411, 316, 320, 321, 635, 639, 649 [IMAGE AVAILABLE]
- 6. 4,769,686, Sep. 6, 1988, Semiconductor device; Masatada Horiuchi, et al., 257/373, 384, 404 [IMAGE AVAILABLE]
- 7. 4,507,673, Mar. 26, 1985, Semiconductor memory device; Masaharu Aoyama, et al., 257/324, 77 [IMAGE AVAILABLE]

1. 5,293,212, Mar. 8, 1994, Non-volatile semiconductor memory device allowing erase of storage data of an arbitrary memory cell and method of erasing data in non-volatile semiconductor memory device; Makoto Yamamoto, et al., 365/218, 185.13, 185.18, 185.26, 185.29, 185.33 [IMAGE AVAILABLE]

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(FILE 'USPAT' ENTERED AT 08:33:55 ON 28 AUG 1998)
L1 242 SEA FLOATING GATE AND CONTROL GATE AND DRAM
L2 1 SEA L1 AND BARRIER ENERGY

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